What is claimed is:

1. A method comprising

receiving a packet comprising one or more sample blocks of a stream, and

discarding any partial sample block of the packet that remains after detecting an end of the packet.

2. The method of claim 1 further comprising

receiving an actual packet length for the packet, and

detecting the end of the packet based upon the actual packet length.

3. The method of claim 1 further comprising detecting the end of the packet in response to receiving a sync signal of the stream.

4. The method of claim 1 further comprising detecting the end of the packet in response to detecting another packet of the stream.

5. The method of claim 1 further comprising

receiving an expected packet length indicative a number of complete sample blocks for the packet,

receiving an actual packet length indicative of a number of complete sample blocks for the packet, and

accepting the number of complete sample blocks indicated by the actual packet length despite the expected packet length indicating fewer complete sample blocks than the actual packet length.

6. The method of claim 1 further comprising

receiving an expected packet length indicative a number of complete sample blocks for the packet,

receiving an actual packet length indicative of a number of complete sample blocks for the packet, and

accepting only the number of complete sample blocks of the packet indicated by the actual packet length despite the expected packet length indicating more complete sample blocks than the actual packet length.

7. The method of claim 1 further comprising transferring only complete sample blocks of the packet to a buffer of a memory.

8. The method of claim 1 further comprising classifying any sample block having less than a defined number of bytes as a partial sample block.

9. An apparatus comprising

a memory interface to access a memory,

a link controller to receive a packet comprising a plurality of sample blocks, and to discard a partial sample block of the packet,

a direct memory access (DMA) controller to receive complete sample blocks from the link controller and to transfer the complete sample blocks to the memory via the memory interface.

10. The apparatus of claim 9 wherein the link controller further classifies any sample block having less than a defined number of bytes as a partial sample block.

11. The apparatus of claim 9 wherein the link controller further

receives a stream identifier for the packet, and

transfers the complete sample blocks to the DMA controller in response to determining that DMA controller has been configured to process streams associated with the stream identifier.

12. The apparatus of claim 9 wherein the link controller

is configured with an expected packet length that is indicative of a number of complete sample blocks expected for each packet of the stream,

receives an actual packet length indicative of a number of complete sample blocks for the packet, and

accepts the number of complete sample blocks indicated by the actual packet length despite the expected packet length indicating fewer complete sample blocks than the actual packet length.

13. The apparatus of claim 9 wherein the link controller

is configured with an expected packet length that is indicative of a number of complete sample blocks expected for each packet of the stream,

receives an actual packet length indicative of a number of complete sample blocks for the packet, and

accepts only the number of complete sample blocks indicated by the actual packet length despite the expected packet length indicating more complete sample blocks than the actual packet length.

14. The apparatus of claim 9 wherein each sample block of the packet comprises at least a first sample for a first audio channel and a second sample for a second audio channel.

15. The apparatus of claim 14 wherein the link controller classifies each sample block having less than a defined number of bytes as a partial sample block.

16. A system comprising a processor, a memory, an audio controller, and an audio codec, wherein

the processor configures the audio controller for processing of a stream of the audio codec by providing the audio controller with a stream identifier for the stream and a sample block length of the stream, and

the audio controller, in response to receiving a packet having the associated steam identifier, classifies sample blocks of the packet based upon the sample block length of the stream, transfers a sample block classified as a complete sample block to the memory, and discards a sample block classified as a partial sample block.

17. The system of claim 16 wherein the audio controller classifies a sample block having less than a number of bytes defined by the sample block length as a partial sample block.

18. The system of claim 16 wherein

the processor allocates a buffer for the stream in the memory, allocates another buffer for another stream in the memory, and configures the audio controller to process the another stream, and

the audio controller transfers a complete sample block of the stream to the buffer for the stream and transfers a complete sample block of the another stream to the another buffer for the another stream.

19. The system of claim 18 wherein the audio controller receives the stream and the another stream from the audio codec.

20. The system of claim 18 wherein the audio controller receives the stream from the audio codec and the another stream from another audio codec.

21. The system of claim 16 wherein

the processor configures the audio controller for the stream by further providing the audio controller with an expected packet length that is indicative of a number of complete sample blocks expected for each packet of the stream, and

the audio controller transfers to the memory a number of complete sample blocks indicated by an actual packet length provided by the audio codec despite the expected packet length indicating fewer complete sample blocks than the actual packet length.

22. The system of claim 16 wherein

the processor configures the audio controller for the stream by further providing the audio controller with an expected packet length that is indicative of a number of complete sample blocks expected for each packet of the stream, and

the audio controller transfers to the memory only a number of complete sample blocks indicated by an actual packet length provided by the audio codec despite the expected packet length indicating more complete sample blocks than the actual packet length.

23. A machine-readable medium comprising a plurality of instructions that in response to being executed result in a device

classifying a plurality of sample blocks of a stream into one or more complete sample blocks and one or more partial sample blocks, and

transferring only the one or more complete sample blocks of the packet to a memory.

24. The machine-readable medium of claim 23 wherein the plurality of instructions in response to being executed further result in the device dropping the one or more partial sample blocks of the packet.

25. The machine-readable medium of claim 24 wherein the plurality of instructions in response to being executed further result in the device transferring a number of complete sample blocks defined by an actual packet length for a packet of the stream despite an expected packet length for the stream indicating fewer complete sample blocks than the actual packet length.

26. The machine-readable medium of claim 23 wherein the plurality of instructions in response to being executed further result in the device transferring only a number of complete sample blocks defined by an actual packet length for a packet of the stream despite an expected packet length for the stream indicating more complete sample blocks than the actual packet length.